ADM-VB630
User Manual

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1 Introduction

The **ADM-VB630** is the base board at the core of the ADK-VB630 Versal AI Edge Development Platform for Space 2.0.

1.1 Key Features

Key Features

- VPX 3U Form Factor
- Supports card depths of 160mm by default, and 220mm via different heatsink options.
- Supports the Versal Edge VE2302 Adaptive SoC device in the 784 pin package
- 1x Banks of space grade DDR4 SDRAM (with ECC)
- Space grade power supply
- Compatible with SpaceVPX Slot profile SLT3-PAY-2F2T-14.2.3
- 2x HSSIO Quads connected to Fat Pipes on VPX P1 connector
- Versatile interface support:
  - Ethernet
  - Spacewire
  - CAN
  - GPIO
  - uSD
  - Dual QSPI
  - UART
- Voltage, current and temperature monitoring
- User LEDs and switches
- Air-cooled and conduction-cooled configurations

1.2 References & Specifications

ANSI/VITA 46.0	*VPX Baseline Standard*, October 2007, VITA, ISBN 1-885731-44-2
ANSI/VITA 46.4	*PCI Express® on the VPX Fabric Connector*, July 2010, VITA, Draft 0.15
ANSI/VITA 46.6	*Gigabit Ethernet Control Plane on VPX*, September 2010, VITA, Draft 0.7
ANSI/VITA 46.11	*System Management on VPX*, June 2015, VITA, ISBN 1-885731-84-1
ANSI/VITA 48.2	*Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to VITA VPX*, July 2010, VITA, ISBN 1-885731-60-4
ANSI/VITA 57.1	*FPGA Mezzanine Card (FMC) Standard*, July 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 65	*OpenVPX™ System Specification*, June 2010, VITA, ISBN 1-885731-58-2
ANSI/VITA 57.4	*FPGA Mezzanine Card Plus(FMC+) Standard*, March 2016, VITA, Draft
ANSI/VITA 78	*Space VPX System*, Feb 2015, VITA, ISBN 1-885731-83-3

Table 1 : References

1.3 Order Code

ADM-VB630(T)

Name	Symbol	Configurations
Configuration	T	/DEV - ADM-VB630/DEV - with XCVE2302 fitted purchasable as part of ADK-VB630 Development Kit /CC4 - build to order with Space Qualified Components /C(x) - build to order with Customer Specific Modifications

Table 2 : Build Options

Not all combinations may be available. Please check with Alpha Data sales for details.

2 Installation

2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2 Hardware Installation

2.2.1 System Requirements

The ADM-VB630 is a 3U Space VPX reference platform for the AMD Versal AI Edge XQVE2302 Adaptable SoC platform for Space 2.0.

Alpha Data offers a Rear Transition Module (RTM) that breaks out all P1 and P2 IO and control lanes (Part number: ADM-VB630-RTM).

2.2.2 Cooling Requirements

The power dissipation of the board is highly dependent on the Adaptive SoC application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with AMD power estimation tools to determine the approximate current requirements for each power rail.

The board is supplied with a passive air cooled or conduction cooled heatsink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and appropriate metalwork for conduction cooled applications.

The board features system monitoring that measures the board and Adaptive SoC temperature. It also includes a self-protection mechanism that will clear the Adaptive SoC configuration if an over-temperature condition is detected.

See Section System Monitoring for health monitoring details.

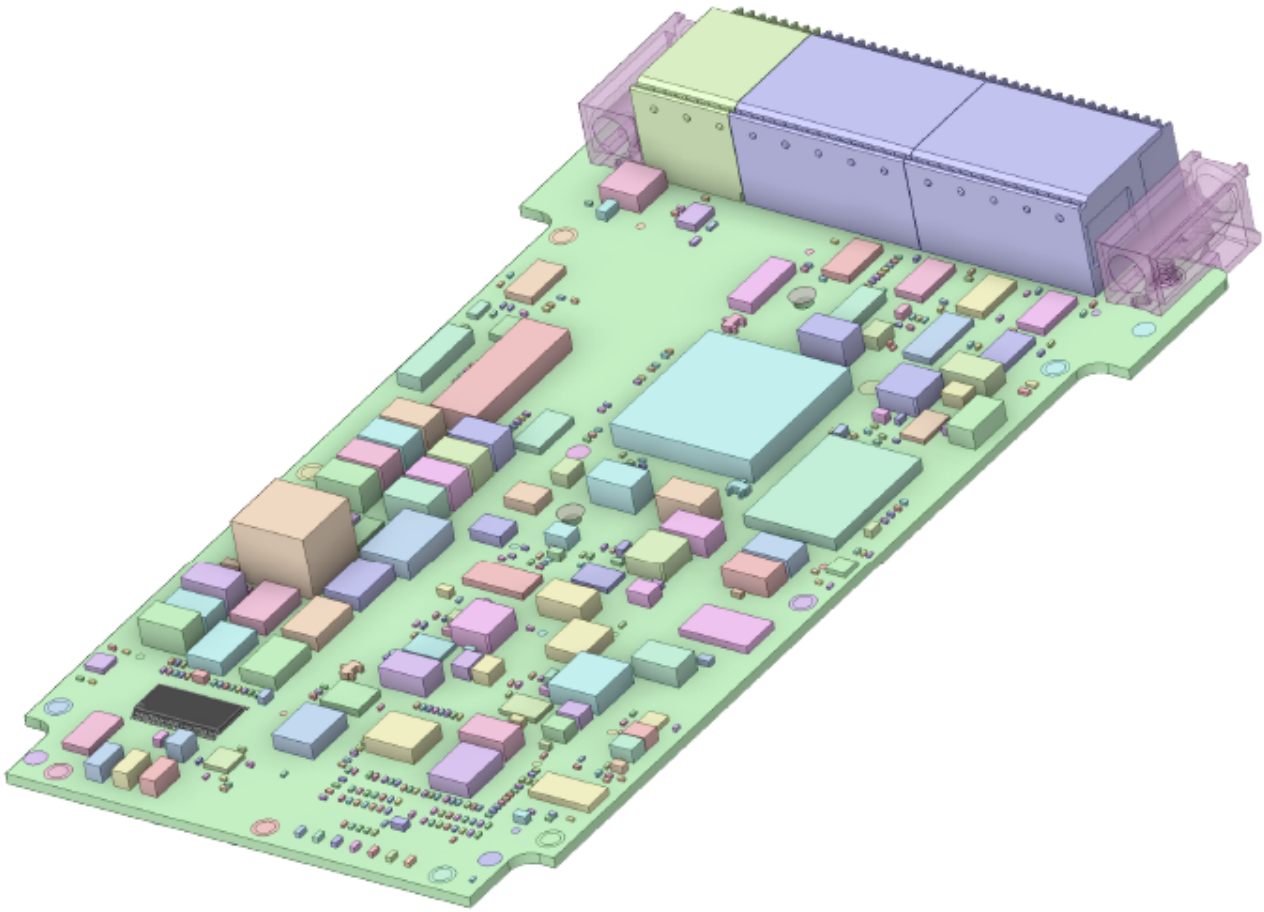

Figure 1 : ADM-VB630

2.3 Software Installation

Please refer to the Reference Designs on the Alpha Data Download Site. Example projects for configuring the Versal Adaptive SoC device and example software for running on the ARM CPUs can be downloaded from there.

2.4 Order Code

See the ADM-VB630 datasheet for complete ordering options.

3 Board Information

3.1 Physical Specifications

The ADM-VB630 complies with vita 78 (3U / 160mm space VPX).

Description	Measure
Total Dy	100.0 mm
Total Dx	160.0 mm
PCB Dx	159.61 mm
Total Dz	20.32 mm
Circuit assembly weight	152 grams
Total weight (with heat sink)	470 grams

Table 3 : Mechanical Dimensions

3.2 Chassis Requirements

3.2.1 Mechanical Requirements

A 3U VPX rack is required for mechanical compatibility. See Appendix E at the end of this document for more information.

3.2.2 Power Requirements

The ADM-VB630 is powered via the +12V VPX power rail, all the internal power rails are generated from this rail.

The ADM-VB630 is capable of drawing up to 6A on the +12V VPX power rail.

The ADM-VB630 also requires the presence of a +3.3V_AUX auxiliary power rail, used to power monitoring and reset circuitry.

The ADM-VB630 is capable of drawing up to 100mA on the +3.3V_AUX power rail, this rail is supplied externally by default but can be generated internally via a build option.

Power consumption estimation requires the use of the AMD XPE spreadsheet (www.xilinx.com/products/technology/power/xpe.html) and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.80	VCC_INT + various	40A
0.92	MGTAVCC	1.5A
1.2	MGTAVTT	3A
1.2	VCCO + DDR4	6A
1.5	VCCO + VCCAUX + VCCAUX_PMC	3A
3.3	VCCO	6A

Table 4 : Available Power By Rail

3.3 Thermal Performance

If the Adaptive SoC core temperature exceeds 105 degrees Celsius, the Adaptive SoC design will be cleared to prevent the card from over-heating.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the AMD Power Estimator (XPE) downloadable at www.xilinx.com/products/technology/power/xpe.html. Download the Versal tool and set the device according to your part number details: Versal AI Edge Series, XCVE2303, SFVA784 package, -2MS speed grade, extended. Set the ambient temperature to your system ambient and select 'user override' for the effective theta JA. Then enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next acquire the VB630 power estimator from Alpha Data by contacting **support@alpha-data.com**. Enter in the power figures from XPE and DRAM utilization into the Alpha Data spreadsheet to get a complete board level estimate.

3.4 Customizations

Alpha Data provides extensive customization options to existing commercial off-the-shelf (COTS) products.

Please contact **sales@alpha-data.com** to obtain a quote and start your project today.

4 Functional Description

4.1 Overview

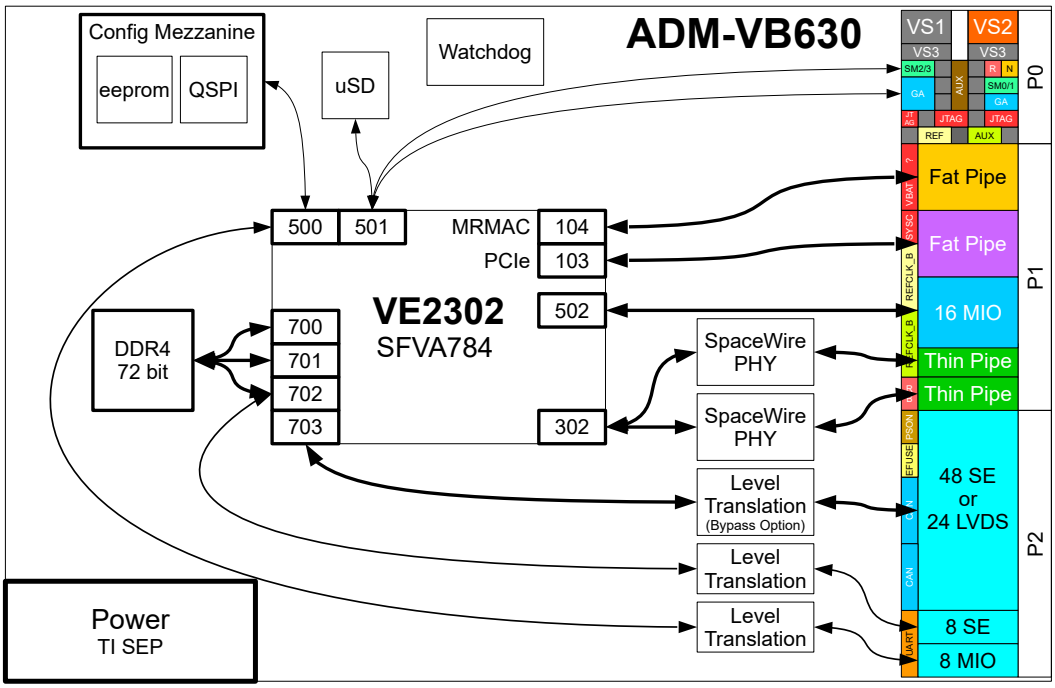

Figure 2 : ADM-VB630 Block Diagram

4.1.1 Switch Definitions

There are two sets of eight DIP switches placed on the bottom of the board. Their functions are described below.

Note:
All switches are OFF by default. Factory Configuration switch must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW1-1	User Switch 1	Pin A10=logic low	Pin A10=logic high
SW1-2	User Switch 2	Pin B11=logic low	Pin B11=logic high
SW1-3	User Switch 3	Pin V21=logic low	Pin V21=logic high
SW1-4	User Switch 4	Pin U22=logic low	Pin U22=logic high
SW1-5	VPX JTAG	Connect JTAG chain to P0	Isolate JTAG chain from P0
SW1-6	Factory Test	-	Normal Operation
SW1-7	Watchdog Enable	-	Normal Operation
SW1-8	Reserved	-	Normal Operation

Table 5 : VPX Control Switch Definitions (SW1)

Switch Ref.	Function	ON State	Off State
SW2-(4:1)	PS_MODE(3:0)	PS Boot Mode - see section Boot Modes	
SW2-5	Hardware Reset	Hardware Reset (complete restart)	Normal Operation
SW2-6	GPIO_EN	VPX GPIO IO Enabled	VPX GPIO IO disabled
SW2-7	VPX_I2C_EN	VPX I2C Enabled	VPX I2C disabled
SW2-8	VPX_IO_EN	VPX MIO IO Enabled	VPX MIO IO disabled

Table 6 : Processor Setup Switch Definitions (SW2)

4.1.2 LED Definitions

There are seven LEDs on the rear of the board which can be used to provide a visual indication of the board status.

Their locations are shown in Figure 3

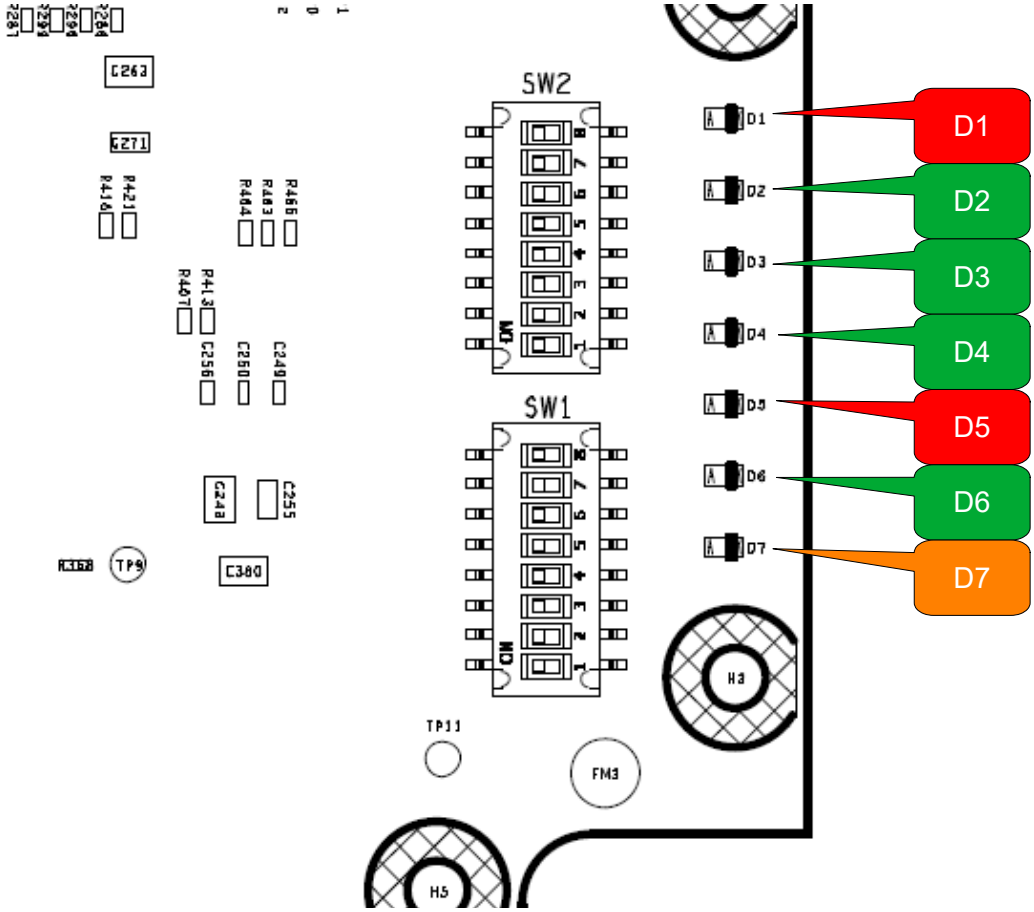

Figure 3 : LED and Switch Locations

There are two LEDs available connected to MIO Bank501 which are intended to be used as system monitor LEDs, See Table 22 # :

Comp. Ref.	Adaptive SoC Pin	Bank	Operation
D1 (Red)	AE9	PL Bank 501	Logic low = LED ON
D2 (Green)	AD9	PL Bank 501	Logic low = LED ON

Table 7 : Sysmon LEDs

There also are two user defined LEDs available:

Comp. Ref.	Adaptive SoC Pin	Bank	Operation
D3 (Green)	B13	PL Bank 302	Logic low = LED ON
D4 (Green)	A14	PL Bank 302	Logic low = LED ON

Table 8 : User Defined LEDs

Comp. Ref.	Function	ON State	Off State
D5 (Red)	PS Error	PS Error	Normal Operation
D6 (Green)	Adaptive SoC (PL) Done	PL is configured	PL is not configured
D7 (Amber)	VPX JTAG STATUS	JTAG chain Connected to VPX P0	JTAG chain isolated from VPX P0

Table 9 : Status LED Definitions

4.2 VPX P0 Interface

4.2.1 SYSRESET#

SYSRESET# is an active low input from the system controller

SYSRESET# is connected to the Adaptive SoC PL side on Bank 302 (Pin F14)(LVCMOS33)

SYSRESET# is connected to the Adaptive SoC PS side PCIe reset pins, LPD_MIO18 and LPD_MIO19 on Bank 502 (Pins W5 and Y6)

4.2.2 AUXCLK

Auxiliary Clock. In OpenVPX this clock line can be used for 1PPS synchronization signaling and is an INPUT to the Adaptive SoC at Bank302 pin D11 (LVCMOS33).

4.2.3 REFCLK

Reference Clock. This clock is an input to the onboard clock distribution and generation system. In OpenVPX this 50MHz clock can be used to align all system clocks.

This clock is an INPUT to the Adaptive SoC at Bank302 pin D10 (LVCMOS33)

4.3 VPX P1 Interfaces

4.3.1 REFCLK1 and REFCLK2

Two further input reference clocks are available.

REFCLK1 is an INPUT to the Adaptive SoC at Bank302 pin C12 (LVCMOS33)

REFCLK2 is an INPUT to the Adaptive SoC at Bank302 pin C10 (LVCMOS33)

4.3.2 PL Interfaces

There are a total of 8 MGT links connected from the Adaptive SoC to the P1 VPX connector.

These links are detailed further in the section Section 4.9.2 below.

The Spacewire interface connects from the HD Bank on the Adaptive SoC to the P1 VPX connector.

4.3.3 PS Interfaces

The following PS interfaces are connected to the P1 VPX connector.

- Ethernet
- UART0

These interfaces are detailed further in the section Section 4.8 below.

4.4 VPX P2 IO

4.4.1 Single Ended PL GPIO[47:0]

6 Bytes of Single Ended GPIO on P2 are routed to/from Adaptive SoC bank 703 and are compatible with 3.3V single ended signals at the VPX connector.

The VCCO of Bank 703 is set to 1.5V.

The Adaptive SoC is protected by a buffer.

4.4.2 Single Ended PL GPIO[55:48]

1 Byte of Single Ended GPIO on P2 is routed to/from Adaptive SoC bank 702 and is compatible with 3.3V single ended signals at the VPX connector.

The VCCO of Bank 702 is set to 1.2V.

The Adaptive SoC is protected by a buffer.

4.4.3 Single Ended PS MIO[23:16]

1 Byte of Single Ended MIO on P2 is routed to/from Adaptive SoC bank 500 and is compatible with 3.3V single ended signals at the VPX connector.

The VCCO of Bank 500 is set to 3.3V.

The Adaptive SoC is protected by a buffer.

4.4.4 PS Interfaces

The following PS interfaces are connected to the P2 VPX connector.

- CAN0
- CAN1
- UART1

These interfaces are detailed further in the section Section 4.8 below.

4.5 JTAG Interface

4.5.1 On-board Interface

A JTAG boundary scan chain is connected to header J2. This allows the connection of the AMD JTAG cable via adapter board AD-JTAG-ADPT2.

Adapter board AD-JTAG-ADPT2 should be inserted into header J2 through the rear of the board, header J2 is keyed to ensure correct orientation.

The scan chain is shown in Figure JTAG Boundary Scan Chain:

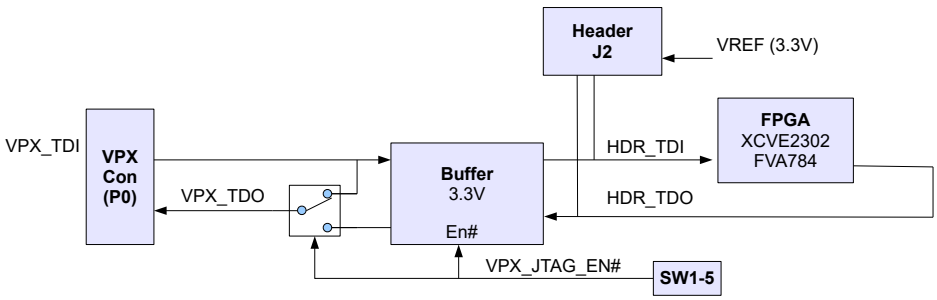

Figure 4 : JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the VPX backplane (SW1-5 is ON), header J2 should not be used.

4.5.2 VPX Interface

The JTAG interface on the VPX backplane is normally unused. When SW1-5 is OFF (default), all JTAG signals to P0 are left floating.

The JTAG interface can be connected to the VPX Backplane (through level-translators) by switching SW1-5 ON.

4.5.3 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The Vcc supply provided on J4 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 350mA.

The JTAG signals at the VPX interface use 3.3V signal levels and are connected through buffers to the on-board scan chain.

4.6 Clocks

The **ADM-VB630** board provides a wide variety of clocking options. The board has 2 programmable frequency clock sources. These clocks can be combined with the Adaptive SoC's internal PLLs to suit a wide variety of communication protocols.

A complete overview of the clock routing on the **ADM-VB630** is given in Clocks. A description of each clock follows.

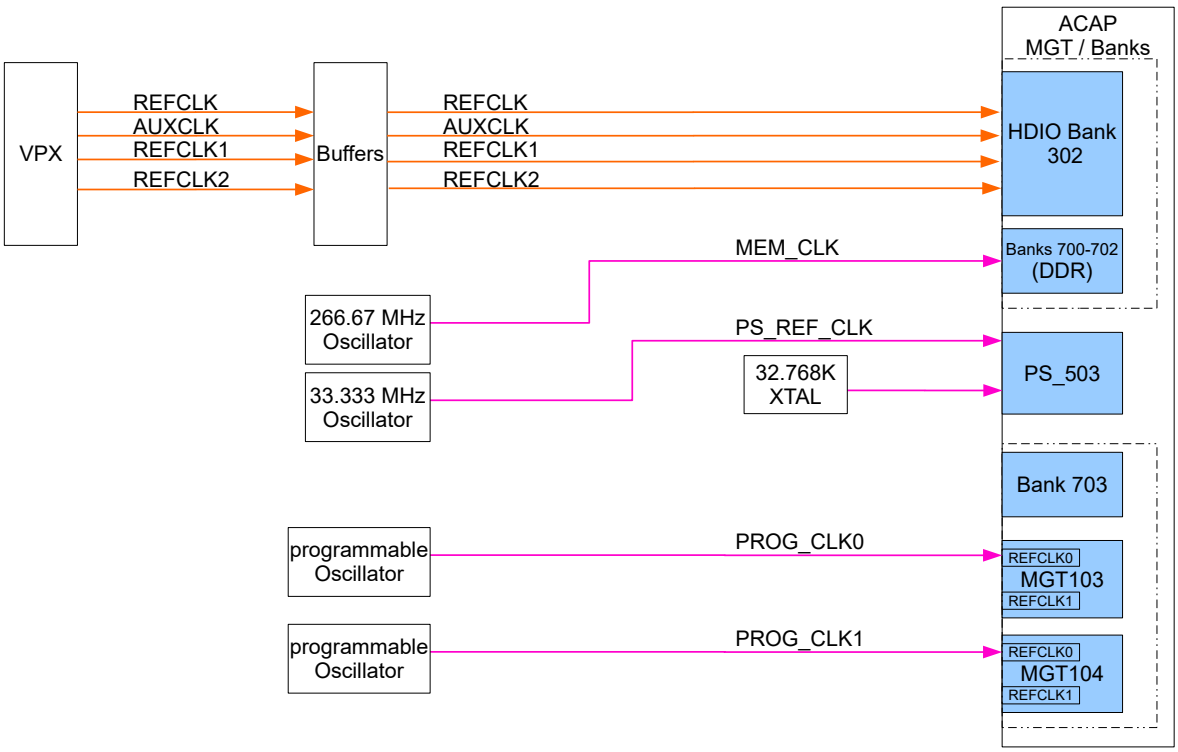

Figure 5 : Clocks

4.6.1 DDR4 Memory Reference Clock (MEM_CLK)

The fixed reference clock MEM_CLK is a differential LVDS15 signal.

MEM_CLK is used as the reference clock for the PL DDR memory logic.

Signal	Frequency	DDR Bank	Target Adaptive SoC Input	IO Standard	"P" pin	"N" pin
MEM_CLK_0	266.67 MHz	0	IO BANK 702	LVDS15	N23	N24

Table 10 : MEM_CLK Connections

4.6.2 Programmable Clock (PROG_CLK)

There is a programable clock source that is forwarded throughout the Adaptive SoC. This clock is programmable through the Alpha Data ADK-VA601 SDK. PROGCLK is generated by a dedicated programmable clock generator IC that offers extremely high frequency resolutions (1ppm increments).

Signal	Frequency	Target Adaptive SoC Input	IO Standard	"P" pin	"N" pin
PROGCLK[0]	Variable	MGTREFCLK0_103	LVDS	M7	M6
PROGCLK[1]	Variable	MGTREFCLK0_104	LVDS	H7	H6

Table 11 : PROGCLK0 Connections

4.6.3 PS_REFCLK

The PS reference clock is an independent 33.333MHz reference clock. This is the master clock of the PS side of the Adaptive SoC.

Signal	Frequency	Adaptive SoC Input	IO Standard	pin
PS_REFCLK	33.333MHz	PS_REF_CLK (Bank 503)	LVCMOS33	U14

Table 12 : PS_REFCLK Connection

4.7 Resets

The Adaptive SoC PS can be reset via switch SW2-5.

Switch	Reset Type	Effect
SW2-5	Power on Reset (PS_POR_B pin)	Clears all logic. Mode pins sampled (i.e. reconfigures hardware). Reboots Adaptive SoC.

Table 13 : Reset Switches

4.8 Adaptive SoC PS Block

4.8.1 Boot Modes

MODE3 (SW2-4)	MODE2 (SW2-3)	MODE1 (SW2-2)	MODE0 (SW2-1)	Boot Mode
ON	ON	ON	ON	JTAG
ON	ON	ON	OFF	Quad SPI (24 bit addressing)
ON	ON	OFF	ON	Quad SPI (32 bit addressing)
ON	OFF	ON	OFF	SD Flash - SD 2.0

Table 14 : Boot Mode Selection

Note: all other possible switch settings are reserved / invalid.

4.8.2 Configuration Daughter Board

The ADM-VB630 board has a socket (J1) that allows custom configuration boards to be used.

The ADM-SDEV-FL1 configuration daughter board is supplied with the ADM-VB630 board as part of the ADK-VA601 development kit.

The ADM-SDEV-FL1 configuration daughter board should be inserted into connector J1.

The ADM-SDEV-FL1 configuration daughter board contains QSPI flash memory which can be used to configure the Adaptive SoC device.

4.8.2.1 QSPI Flash Memory

The ADM-SDEV-FL1 board has 2x 1Gb (128MB) quad-QSPI Flash devices. These can be interfaced in x1,x2,x4 or x8 mode.

See MIO Map

4.8.2.2 MicroSD Card

The ADM-VB630 board has a MicroSD card socket (SD 2.0 standard at 3.3V).

See MIO Map

4.8.3 Ethernet RGMII Interface

This interface is accessible at the VPX P1 connector.

The Gigabit Ethernet Manager (GEM0) connects to a phy on the ADM-VB630_RTM via RGMII and MDIO interfaces.

See MIO Map

4.8.4 UART interfaces

The UART0 interface is routed through to the VPX P1 connector. See MIO Map

The UART0 interface operates at 3.3V switching levels.

The UART1 interface is routed through to the VPX P2 connector. See MIO Map

The UART1 interface operates at 3.3V switching levels.

See MIO Map

4.8.5 CAN interfaces

Two CAN interfaces are routed to Rad hard transceiver chips on the board.

Signal	Bank	Type	IO Standard
CAN0_TX	502	MIO	LVCMOS33
CAN0_RX	502	MIO	LVCMOS33
CAN1_TX	502	MIO	LVCMOS33
CAN1_RX	502	MIO	LVCMOS33

Table 15 : CAN PL side connections

The other sides of the CAN transceivers are routed out to the VPX P2 connector.

4.9 Adaptive SoC PL Side

4.9.1 I/O Bank Voltages

The Adaptive SoC IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in PL Adaptive SoC IO Banks.

IO Banks	Voltage	Purpose
700, 701, 702	1.2V	DDR4
703	1.5V	VPX P2 GPIO
302	3.3V	Spacewire and VPX Clocks

Table 16 : PL Adaptive SoC IO Banks

4.9.2 PL MGT Links

There are a total of 8 Multi-Gigabit Transceiver (MGT) links connected to the Adaptive SoC. These are connected as follows:

Links	Banks	Width	Max Rate	Connection
VPX_P1_HSSIO(7:0)	103, 104	8	16Gbps	VPX P1 Connector Data Planes (2 fat pipes)

Table 17 : PL MGT Links

4.9.3 VPX P2 GPIO Interface

The P2 VPX Connector has GPIO connections arranged into byte wide lanes as follows:

Group	Adaptive SoC Bank	Name	Function
GPIO_1V5	703	GPIO(47:0)	6 bytes x8 single-ended
GPIO_1V2	702	GPIO(55:48)	1 bytes x8 single-ended

Table 18 : VPX P2 GPIO Groups

4.9.4 VPX GPIO Buffers

The VPX Connector GPIO connections are buffered by byte wide SN54SLC8T245-SEP bidirectional buffers.

Each byte lane buffer has a dedicated output enable pin and a direct control pin.

Name	Function
OE_L	Output Enable : 0=ENABLED 1=DISABLED
DIR	Direction Control : 0=INPUT 1=OUTPUT

Table 19 : Buffer Pins

4.9.5 DDR4 Memory

One bank of DDR4 SDRAM memory is soldered down to the board. The available density of the memory is 8GB. The memory interface is 72-bit wide data (64 data + 8 ECC). Maximum signaling rate is 2133 MT/s.

Memory solutions are available from AMD (See AMD PG313 Versal Adaptive SoC Programmable Network on Chip and Integrated Memory Controller v1.0). All pin location information is included in DDR4 Pinout Table.

The components used are Teledyne e2v DDR4PT08G72AZR1B or equivalent.

4.10 System Monitoring

The **VB630** has the ability to monitor temperature and voltage to maintain a check on the operation of the board.

The Adaptive SoC can monitor its own rails internally and in addition can monitor the following:

Monitor	*Purpose*
12V0	12V Board Input Supply Current - MIO48 pin AD10
2V5_DIG	2.5V Supply Voltage - MIO49 pin AC10
Temp(2..0)	TMP9R01-SEP internal temperatures (3 devices)
Temp(5..3)	pcb temperatures (3 different points - measured by TMP9R01-SEP devices)

Table 20 : Voltage and Temperature Monitoring Points

4.10.1 Automatic Temperature Monitoring

The system monitor checks that the board and Adaptive SoC are being operated within the specified limits. If the temperature is close to the limit, a "Warning Alarm" interrupt is set.

If a limit is exceeded, a "Critical Alarm" interrupt is set. After the Critical Alarm is set, there is a 5 second delay before the system monitor unconfigures the Adaptive SoC by asserting its "POR_B" pin.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

The temperature limits are shown in Table Temperature Limits. Note that the Min and Max values include a 5°C margin to prevent measurement errors triggering a false alarm.

	Adaptive SoC				Board			
	Min	Lower Warning	Upper Warning	Max	Min	Lower Warning	Upper Warning	Max
Extended	-5°C	+5°C	+95°C	+105°C	-5°C	+5°C	+80°C	+90°C
Industrial	-45°C	-35°C	+95°C	+105°C	-45°C	-35°C	+80°C	+90°C
Military	-60°C	-50°C	+140°C	+170°C	-60°C	-50°C	+125°C	+135°C

Table 21 : Temperature Limits

4.10.2 System Monitor Status LEDs

If enabled for this function, LEDs D2 (Green) and D1 (Red) indicate the sysmon status.

LEDs	*Status*
Flashing Green + Flashing Red (alternate)	Service Mode
Red	Missing application firmware or invalid firmware
Red + Green	Standby (Powered off)
Green	Running and no alarms
Flashing Green + Red	Attention - alarm active
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Red	Adaptive SoC configuration cleared to protect board

Table 22 : System Monitor Status LEDs

4.11 Configuration

There are three main ways of configuring the Adaptive SoC on the ADM-VB630:

- From QSPI Flash memory, at power-on, as described in Section 4.11.1
- From uSD Flash memory, at power-on, as described in Section 4.11.2
- Using USB cable connected at either USB port Section 4.11.3

4.11.1 Configuration From QSPI Flash Memory

The Adaptive SoC can be automatically configured at power-on from two 1 Gbit QSPI flash memory devices configured as an x8 dual parallel SPI device (2x Micron part number MT25QL01GBBB8E12).

At power-on, the Adaptive SoC attempts to configure itself automatically according to the mode pins as described in Section 4.8.1. If the mode is set to QSPI24 or QSPI32, the Adaptive SoC will search on the header of the binary that has been flashed into the card. This normally results in SPIx8 configuration.

4.11.1.1 Building and Programming QSPI Configuration Images

Example Vivado projects(.xpr format) are available in the downloads area for the ADK-VB630. Access should be requested via email to: **support@alpha-data.com**

Below are described the steps to do QSPI Flash programming.

- Connect the ADM-VB630 to a VPX system
- Ensure ADM-VB630 switches SW2-1, SW2-2, SW2-3, SW2-4 are all ON (see Switch Definitions)
- Set ADM-VB630 SW1-5 to ON to switch the JTAG chain through to the ADM-VA600-RTM (see Switch Definitions)
- Connect the download cable between the test PC and the JTAG programming header on the ADM-VA600-RTM (J29)

The flash programming commands are run via Vivado as follows:

- Open Vivado -> Open Project(select .xpr file) -> Select HW Manager -> Open Target -> Auto Connect
- Right click on xcve2302_1 -> Add Configuration Memory Device -> search for 'cfgmem-qspi-x8-dual_parallel', selecting it -> click OK
- A message asking the user to configure the device now will pop up. Click OK accepting it
- Now, copy the path to the PDI image in the 'Initialization PDI' field, and click OK. This will program the QSPI Flash with the example design that you have opened. If you have a .BIN file instead, use the path for that binary file and leave the other fields as are

If you followed the previous steps, the Adaptive SoC should have been correctly configured. To verify this, power off the ADM-VB630, set switches SW2-1, SW2-3, SW2-4 ON and SW2-2 OFF. Then power up the ADM-VB630. Both the DONE_L and STAT_0 LEDs should illuminate after a few seconds(see LED Definitions)

4.11.2 Configuration From uSD Flash Memory

The Adaptive SoC can be automatically configured at power-on from the Micro Secure Digital card (uSD) in the centre of the board.

The ADM-VB630 is shipped with a simple bitstream. On request, Alpha Data can pre-load custom bitstreams during production test. Please contact **sales@alpha-data.com** in order to discuss this possibility.

At power-on, the Adaptive SoC attempts to configure itself automatically according to the mode pins as described in Section 4.8.1. Alpha Data ships these cards set to the uSD boot mode by default.

4.11.2.1 Building and Programming uSD Configuration Images

Find below the steps to get a bootable image file(BOOT.BIN) from your implemented example design,

- Prepare the uSD card by formatting it as a whole FAT partition.

- Find the generated PDI file of your design(implementation folder of the project).
- Copy the .pdi to FAT32 SD card and rename it to BOOT.bin

The uSD card is now ready to be booted from. It can be inserted in the ADM-VB630 with the appropriate boot switch setting. The example design will be programmed into the Adaptive SoC automatically at boot.

4.11.3 Configuration via JTAG

An AMD-Xilinx download Cable may be attached to the JTAG download header on the ADM-VB630-RTM. This permits the Adaptive SoC to be reconfigured using the Xilinx Vivado Hardware Manager. The device will be automatically recognized in Vivado Hardware Manager and Vitis.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of AMD UG908

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Appendix A: P1 Pin Assignments

Appendix A.1: Data Plane 1 (P1 Wafers 1-4)

Signal	VPX P1	ACAP	|	ACAP	VPX P1	Signal
P1_TX0_N	E1	N4	|	P1	B1	P1_RX0_N
P1_TX0_P	D1	N5	|	P2	A1	P1_RX0_P
P1_TX1_N	F2	L4	|	M1	C2	P1_RX1_N
P1_TX1_P	E2	L5	|	M2	B2	P1_RX1_P
P1_TX2_N	E3	J4	|	K1	B3	P1_RX2_N
P1_TX2_P	D3	J5	|	K2	A3	P1_RX2_P
P1_TX3_N	F4	G4	|	H1	C4	P1_RX3_N
P1_TX3_P	E4	G5	|	H2	B4	P1_RX3_P

Table 23 : Data Plane 1 (P1 Wafers 1-4)

Appendix A.2: Data Plane 2 (P1 Wafers 5-8)

Signal	VPX P1	ACAP	|	ACAP	VPX P1	Signal
P1_TX4_N	E5	E4	|	F1	B5	P1_RX4_N
P1_TX4_P	D5	E5	|	F2	A5	P1_RX4_P
P1_TX5_N	F6	D7	|	D1	C6	P1_RX5_N
P1_TX5_P	E6	D8	|	D2	B6	P1_RX5_P
P1_TX6_N	E7	C4	|	B1	B7	P1_RX6_N
P1_TX6_P	D7	C5	|	B2	A7	P1_RX6_P
P1_TX7_N	F8	B7	|	A4	C8	P1_RX7_N
P1_TX7_P	E8	B8	|	A5	B8	P1_RX7_P

Table 24 : Data Plane 2 (P1 Wafers 5-8)

Appendix A.3: Ethernet Pins (P1 Wafers 9-11)

Signal	VPX P1	|	VPX P1	Signal
RGMII_RXD0	A9	|	A11	RGMII_TXD0
RGMII_RXD1	B9	|	B11	RGMII_TXD1
RGMII_RXD2	D9	|	D11	RGMII_TXD2
RGMII_RXD3	E9	|	E11	RGMII_TXD3
RGMII_RX_CTRL	B10	|	E10	RGMII_TX_CTRL
RGMII_RX_CLK	C10	|	F10	RGMII_TX_CLK
RGMII_MDIO_CLK	E12	|	F12	RGMII_MDIO_DAT

Table 25 : Ethernet (P1 Wafers 9-11)

Appendix A.4: UART0 Interface (P1 Wafer 12)

Signal (DIFF)	VPX P1	ACAP		ACAP	VPX P1	Signal (DIFF)
UART0_TXD	B12	V5		U5	C12	UART0_RXD

Table 26 : SpaceWire Interface (P1 Wafer 12)

Appendix A.5: SpaceWire Interface (P1 Wafers 13-16)

Signal (DIFF)	VPX P1	ACAP (SE)		ACAP (SE)	VPX P1	Signal (DIFF)
SPW01_DOUT_N	F16	D14		E14	C16	SPW01_DIN_N
SPW01_DOUT_P	E16	-		-	B16	SPW01_DIN_P
SPW02_DOUT_N	F14	E12		C14	C14	SPW02_DIN_N
SPW02_DOUT_P	E14	-		-	B14	SPW02_DIN_P
SPW01_SOUT_N	E15	D12		C13	B15	SPW01_SIN_N
SPW01_SOUT_P	D15	-		-	A15	SPW01_SIN_P
SPW02_SOUT_N	E13	F11		E13	B13	SPW02_SIN_N
SPW02_SOUT_P	D13	-		-	A13	SPW02_SIN_P

Table 27 : SpaceWire Interface (P1 Wafers 13-16)

Appendix B: P2 Pin Assignments

Appendix B.1: GPIO (P2 Wafers 1-14)

Signal	VPX P2	ACAP		ACAP	VPX P2	Signal
GPIO<0>	A1	J27	|	C23	B8	GPIO<28>
GPIO<1>	B1	H28	|	B23	C8	GPIO<29>
GPIO<2>	D1	H27	|	A23	E8	GPIO<30>
GPIO<3>	E1	G28	|	A24	F8	GPIO<31>
GPIO<4>	B2	G27	|	G21	A9	GPIO<32>
GPIO<5>	C2	F28	|	H22	B9	GPIO<33>
GPIO<6>	E2	E27	|	E20	D9	GPIO<34>
GPIO<7>	F2	E28	|	F21	E9	GPIO<35>
GPIO<8>	A3	C27	|	D20	B10	GPIO<36>
GPIO<9>	B3	B28	|	D21	C10	GPIO<37>
GPIO<10>	D3	H25	|	B20	E10	GPIO<38>
GPIO<11>	E3	J26	|	C21	F10	GPIO<39>
GPIO<12>	B4	G25	|	C22	A11	GPIO<40>
GPIO<13>	C4	G26	|	B22	B11	GPIO<41>
GPIO<14>	E4	F26	|	F23	D11	GPIO<42>
GPIO<15>	F4	E26	|	F24	E11	GPIO<43>
GPIO<16>	A5	C25	|	E24	B12	GPIO<44>
GPIO<17>	B5	B25	|	F25	C12	GPIO<45>
GPIO<18>	D5	A25	|	D25	E12	GPIO<46>
GPIO<19>	E5	A26	|	D26	F12	GPIO<47>
GPIO<20>	B6	B26	|	R21	A13	GPIO<48>
GPIO<21>	C6	B27	|	P22	B13	GPIO<49>
GPIO<22>	E6	H23	|	N21	D13	GPIO<50>
GPIO<23>	F6	H24	|	M21	E13	GPIO<51>
GPIO<24>	A7	E22	|	K21	B14	GPIO<52>
GPIO<25>	B7	E23	|	L22	C14	GPIO<53>
GPIO<26>	D7	D24	|	J21	E14	GPIO<54>
GPIO<27>	E7	C24	|	J22	F14	GPIO<55>
GPIO_DIR0	-	D27	|	A20	-	GPIO_DIR4
GPIO_DIR1	-	C28	|	A21	-	GPIO_DIR5
GPIO_DIR2	-	F22	|	R22	-	GPIO_DIR6
GPIO_DIR3	-	G23	|	T21	-	GPIO_OE_L

Table 28 : GPIO (P2 Wafers 1-14) (continued on next page)

Signal	VPX P2	ACAP		ACAP	VPX P2	Signal
GPIO_DIR2_<0>	-	L24	|	N25	-	GPIO_DIR2_<2>
GPIO_DIR2_<1>	-	L25	|	M25	-	GPIO_DIR2_<3>

Table 28 : GPIO (P2 Wafers 1-14)

Appendix B.2: MIO (P2 Wafers 15-16)

Signal	Dir	VPX P2	ACAP		ACAP	VPX P2	Dir	Signal
MIO<16>	IO	A15	AF3	|	AF4	B16	IO	MIO<20>
MIO<17>	IO	B15	AG3	|	AE4	C16	IO	MIO<21>
MIO<18>	IO	D15	AH3	|	AD4	E16	IO	MIO<22>
MIO<19>	IO	E15	AH4	|	AC4	F16	IO	MIO<23>
MIO_DIR1	n/a	-	AA4	|	Y4	-	n/a	MIO_DIR2

Table 29 : MIO (P2 Wafers 15-16)

Appendix B.3: Serial Interfaces (P2 G column)

Signal	VPX P2	Notes
UART1_RXD	G15	UART1 RX
UART1_TXD	G13	UART1 TX
CAN0H	G5	CAN BUS0 H
CAN0L	G7	CAN BUS0 L
CAN1H	G9	CAN BUS1 H
CAN1L	G11	CAN BUS1 L

Table 30 : Serial (P2 G column)

Appendix C: MIO Map

Pin Number	Pin Name	Signal Name	Comment
AA1	PMC_MIO0_500	QSPI0_CLK	Dual-Parallel Quad SPI
AB1	PMC_MIO1_500	QSPI0_IO[1]	Dual-Parallel Quad SPI
AD1	PMC_MIO2_500	QSPI0_IO[2]	Dual-Parallel Quad SPI
AE1	PMC_MIO3_500	QSPI0_IO[3]	Dual-Parallel Quad SPI
AF1	PMC_MIO4_500	QSPI0_IO[0]	Dual-Parallel Quad SPI
AG1	PMC_MIO5_500	QSPI0_CS_b	Dual-Parallel Quad SPI
AH2	PMC_MIO6_500	PMC_MIO_500_6	GPIO to Config Socket
AG2	PMC_MIO7_500	QSPI1_CS_b	Dual-Parallel Quad SPI
AE2	PMC_MIO8_500	QSPI1_IO[0]	Dual-Parallel Quad SPI
AD2	PMC_MIO9_500	QSPI1_IO[1]	Dual-Parallel Quad SPI
AC2	PMC_MIO10_500	QSPI1_IO[2]	Dual-Parallel Quad SPI
AB2	PMC_MIO11_500	QSPI1_IO[3]	Dual-Parallel Quad SPI
AA3	PMC_MIO12_500	QSPI1_CLK	Dual-Parallel Quad SPI
AB3	PMC_MIO13_500	UNUSED	UNUSED
AC3	PMC_MIO14_500	MSKRST_L_IN	VPX reset mask
AE3	PMC_MIO15_500	VPX_I2C_EN_L	VPX I2C Enable
AF3	PMC_MIO16_500	PMC_GPIO16	PMC GPIO to VPX
AG3	PMC_MIO17_500	PMC_GPIO17	PMC GPIO to VPX
AH3	PMC_MIO18_500	PMC_GPIO18	PMC GPIO to VPX
AH4	PMC_MIO19_500	PMC_GPIO19	PMC GPIO to VPX
AF4	PMC_MIO20_500	PMC_GPIO20	PMC GPIO to VPX
AE4	PMC_MIO21_500	PMC_GPIO21	PMC GPIO to VPX
AD4	PMC_MIO22_500	PMC_GPIO22	PMC GPIO to VPX
AC4	PMC_MIO23_500	PMC_GPIO23	PMC GPIO to VPX
AA4	PMC_MIO24_500	PMC_DIR1	GPIO buffer Direction control
Y4	PMC_MIO25_500	PMC_DIR2	GPIO buffer Direction control
AA5	PMC_MIO26_501	SD0_CLK	SDCARD
AB5	PMC_MIO27_501	PMC_MIO_500_27	GPIO to Config Socket
AC5	PMC_MIO28_501	UNUSED	UNUSED
AD5	PMC_MIO29_501	SD0_CMD	SDCARD
AE6	PMC_MIO30_501	SD0_DATA0	SDCARD
AD6	PMC_MIO31_501	SD0_DATA1	SDCARD
AB6	PMC_MIO32_501	SD0_DATA2	SDCARD
AA6	PMC_MIO33_501	SD0_DATA3	SDCARD

Table 31 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
AB7	PMC_MIO34_501	UNUSED	UNUSED
AC7	PMC_MIO35_501	UNUSED	UNUSED
AD7	PMC_MIO36_501	VPX_GA_IN0	VPX Signal
AE7	PMC_MIO37_501	VPX_GA_IN1	VPX Signal
AE8	PMC_MIO38_501	VPX_GA_IN2	VPX Signal
AC8	PMC_MIO39_501	VPX_GA_IN3	VPX Signal
AB8	PMC_MIO40_501	VPX_GA_IN4	VPX Signal
AA8	PMC_MIO41_501	VPX_GAP_IN	VPX Signal
AA9	PMC_MIO42_501	NVMRO_IN	VPX Signal
AC9	PMC_MIO43_501	SYSCON_L_IN	VPX Signal
AD9	PMC_MIO44_501	GREEN LED	Sysmon LED
AE9	PMC_MIO45_501	RED LED	Sysmon LED
AF9	PMC_MIO46_501	WDOG_PS	Watchdog signal
AF10	PMC_MIO47_501	nWDOG_EN	Watchdog Enable
AD10	PMC_MIO48_501	VPWR_CURRENT	12V Current sense
AC10	PMC_MIO49_501	2V5_DIG	2V5 rail sense
AB10	PMC_MIO50_501	GEM0_MDIO_CLK	GEM0 Ethernet
AA10	PMC_MIO51_501	GEM0_MDIO_DATA	GEM0 Ethernet
T1	LPD_MIO0_502	GEM0_TX_CLK	GEM0 Ethernet
U1	LPD_MIO1_502	GEM0_TX_DATA[0]	GEM0 Ethernet
W1	LPD_MIO2_502	GEM0_TX_DATA[1]	GEM0 Ethernet
Y1	LPD_MIO3_502	GEM0_TX_DATA[2]	GEM0 Ethernet
Y2	LPD_MIO4_502	GEM0_TX_DATA[3]	GEM0 Ethernet
W2	LPD_MIO5_502	GEM0_TX_CTRL	GEM0 Ethernet
V2	LPD_MIO6_502	GEM0_RX_CLK	GEM0 Ethernet
U2	LPD_MIO7_502	GEM0_RXD0	GEM0 Ethernet
T3	LPD_MIO8_502	GEM0_RXD1	GEM0 Ethernet
U3	LPD_MIO9_502	GEM0_RXD2	GEM0 Ethernet
V3	LPD_MIO10_502	GEM0_RXD3	GEM0 Ethernet
Y3	LPD_MIO11_502	GEM0_RX_CTRL	GEM0 Ethernet
W4	LPD_MIO12_502	UART1_TXD_MIO	UART1
V4	LPD_MIO13_502	UART1_RXD_MIO	UART1
T4	LPD_MIO14_502	CAN0_RX	CAN Interface 0
T5	LPD_MIO15_502	CAN0_TX	CAN Interface 0
U5	LPD_MIO16_502	UART0_RXD_MIO	UART0
V5	LPD_MIO17_502	UART0_TXD_MIO	UART0

Table 31 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
W5	LPD_MIO18_502	PERST_PL_L	Reset Input
Y6	LPD_MIO19_502	PERST_PL_L	Reset Input
W6	LPD_MIO20_502	VPX_PS_SCL	VPX I2C SCL
U6	LPD_MIO21_502	VPX_PS_SDA	VPX I2C SDA
T6	LPD_MIO22_502	I2C0_SCL	I2C to Config socket
Y7	LPD_MIO23_502	I2C0_SDA	I2C to Config socket
Y8	LPD_MIO24_502	CAN1_TX	CAN Interface 1
Y9	LPD_MIO25_502	CAN1_RX	CAN Interface 1

Table 31 : MIO Map

Appendix D: DDR4 Pinout Table

Pin Number	Signal Name	ACAP Bank
AB12	DDR4_0_A<0>	700
AE22	DDR4_0_A<1>	700
AB17	DDR4_0_A<10>	700
AE13	DDR4_0_A<11>	700
AH12	DDR4_0_A<12>	700
AD15	DDR4_0_A<13>	700
AD21	DDR4_0_A<14>	700
AD17	DDR4_0_A<15>	700
AD22	DDR4_0_A<2>	700
AB15	DDR4_0_A<3>	700
AD12	DDR4_0_A<4>	700
AE17	DDR4_0_A<5>	700
AD16	DDR4_0_A<6>	700
AG11	DDR4_0_A<7>	700
AE14	DDR4_0_A<8>	700
AB14	DDR4_0_A<9>	700
AC11	DDR4_0_ACT_N	700
AC25	DDR4_0_ALERT_N	701
AC16	DDR4_0_BA0	700
AD11	DDR4_0_BA1	700
AB18	DDR4_0_BG0	700
AE18	DDR4_0_BG1	700
AB21	DDR4_0_CKE	700
AD19	DDR4_0_CLK_C	700
AC19	DDR4_0_CLK_T	700
AC17	DDR4_0_CS_N	700
AB27	DDR4_0_DEBUG	701
AD24	DDR4_0_DM<0>	701
AE28	DDR4_0_DM<1>	701
AH13	DDR4_0_DM<2>	700
AG12	DDR4_0_DM<3>	700
V28	DDR4_0_DM<4>	701
V22	DDR4_0_DM<5>	701
N28	DDR4_0_DM<6>	702

Table 32 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank
U25	DDR4_0_DM<7>	702
U23	DDR4_0_DM<8>	702
AD25	DDR4_0_DQ<0>	701
AF25	DDR4_0_DQ<1>	701
AG28	DDR4_0_DQ<10>	701
AE27	DDR4_0_DQ<11>	701
AH27	DDR4_0_DQ<12>	701
AD26	DDR4_0_DQ<13>	701
AE26	DDR4_0_DQ<14>	701
AF26	DDR4_0_DQ<15>	701
AH18	DDR4_0_DQ<16>	700
AH17	DDR4_0_DQ<17>	700
AH22	DDR4_0_DQ<18>	700
AH15	DDR4_0_DQ<19>	700
AH25	DDR4_0_DQ<2>	701
AH20	DDR4_0_DQ<20>	700
AG22	DDR4_0_DQ<21>	700
AH14	DDR4_0_DQ<22>	700
AG21	DDR4_0_DQ<23>	700
AG13	DDR4_0_DQ<24>	700
AG18	DDR4_0_DQ<25>	700
AE19	DDR4_0_DQ<26>	700
AG15	DDR4_0_DQ<27>	700
AF14	DDR4_0_DQ<28>	700
AF18	DDR4_0_DQ<29>	700
AH24	DDR4_0_DQ<3>	701
AF13	DDR4_0_DQ<30>	700
AF19	DDR4_0_DQ<31>	700
AB26	DDR4_0_DQ<32>	701
W27	DDR4_0_DQ<33>	701
AA26	DDR4_0_DQ<34>	701
Y26	DDR4_0_DQ<35>	701
V25	DDR4_0_DQ<36>	701
W26	DDR4_0_DQ<37>	701
AA28	DDR4_0_DQ<38>	701
AB28	DDR4_0_DQ<39>	701

Table 32 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank
AE24	DDR4_0_DQ<4>	701
V24	DDR4_0_DQ<40>	701
Y23	DDR4_0_DQ<41>	701
W25	DDR4_0_DQ<42>	701
V23	DDR4_0_DQ<43>	701
Y22	DDR4_0_DQ<44>	701
AA22	DDR4_0_DQ<45>	701
W24	DDR4_0_DQ<46>	701
AA21	DDR4_0_DQ<47>	701
P27	DDR4_0_DQ<48>	702
R27	DDR4_0_DQ<49>	702
AG25	DDR4_0_DQ<5>	701
K28	DDR4_0_DQ<50>	702
R28	DDR4_0_DQ<51>	702
T28	DDR4_0_DQ<52>	702
K27	DDR4_0_DQ<53>	702
M27	DDR4_0_DQ<54>	702
L28	DDR4_0_DQ<55>	702
K26	DDR4_0_DQ<56>	702
T26	DDR4_0_DQ<57>	702
L26	DDR4_0_DQ<58>	702
T25	DDR4_0_DQ<59>	702
AG23	DDR4_0_DQ<6>	701
J25	DDR4_0_DQ<60>	702
R26	DDR4_0_DQ<61>	702
P25	DDR4_0_DQ<62>	702
M26	DDR4_0_DQ<63>	702
K24	DDR4_0_DQ<64>	702
T23	DDR4_0_DQ<65>	702
K23	DDR4_0_DQ<66>	702
L23	DDR4_0_DQ<67>	702
R24	DDR4_0_DQ<68>	702
P24	DDR4_0_DQ<69>	702
AH23	DDR4_0_DQ<7>	701
R23	DDR4_0_DQ<70>	702
J24	DDR4_0_DQ<71>	702

Table 32 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank
AG26	DDR4_0_DQ<8>	701
AG27	DDR4_0_DQ<9>	701
AF23	DDR4_0_DQS0_C	701
AF24	DDR4_0_DQS0_T	701
AD27	DDR4_0_DQS1_C	701
AC28	DDR4_0_DQS1_T	701
AH19	DDR4_0_DQS2_C	700
AG20	DDR4_0_DQS2_T	700
AG16	DDR4_0_DQS3_C	700
AG17	DDR4_0_DQS3_T	700
Y27	DDR4_0_DQS4_C	701
Y28	DDR4_0_DQS4_T	701
AA23	DDR4_0_DQS5_C	701
Y24	DDR4_0_DQS5_T	701
U28	DDR4_0_DQS6_C	702
U27	DDR4_0_DQS6_T	702
N27	DDR4_0_DQS7_C	702
P26	DDR4_0_DQS7_T	702
M23	DDR4_0_DQS8_C	702
M22	DDR4_0_DQS8_T	702
AC22	DDR4_0_ODT	700
AD14	DDR4_0_PARITY	700
AC13	DDR4_0_RAS_N	700
AC24	DDR4_0_RESET_N	701
N24	MEM_CLK_0_PIN_N	702
N23	MEM_CLK_0_PIN_P	702

Table 32 : DDR4 Pinout Table

Appendix E: VPX Chassis Information

E.1 VPX Chassis Requirements

It is strongly recommended to install the ADM-VB630 board and RTM within a VPX chassis.

The minimum chassis requirements for use with the ADM-VB630/DEV are listed below:

- Chassis Height : 3U
- Slot type : Air cooled
- Depth : 160mm deep
- Backplane : Straight through power/ground (25G pass through)
- PSU : 300W

There are many configurations of chassis available from various manufacturers, such as Elma and Kontron/ Hartmann.

(An example of a suitable chassis is Elma model number: 39E01BWX6ZY2VCC0-T2).

Revision History

Date	Revision	Nature of Change
21 Oct 2024	0.1	Initial Draft
06 Nov 2024	0.2	Fixed error in PSU table
15 Nov 2024	0.3	Updated block diagram
07 Jan 2025	1.0	First release after review
05 May 2025	1.1	Added information on weights and VPX chassis

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